

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Mark Moshayed) Group Art Unit 2811
App. No. : 09/514,633)
Filed : February 28, 2000)
For : APPARATUS FOR STACKING)
SEMICONDUCTOR CHIPS)
Examiner : Jhihan B. Clark)

#2

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Enclosed is form PTO-1449 listing references that are also enclosed. This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required in accordance with 37 C.F.R. § 1.97(b)(3). If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410. A duplicate copy of this Statement is enclosed for that purpose.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 3/21/01

By: John R. King
John R. King
Registration No. 34,362
Attorney of Record
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FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. SIMTECH.088RAC	APPLICATION NO. 09/514,633
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)		APPLICANT Mark Moshayedi	
		FILING DATE February 28, 2000	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		3,246,386	04/1966	Ende			
		3,290,559	12/1966	Kirby, et al.			
		3,313,986	04/1967	Kilby			
		3,377,516	04/1968	Ellett, et al.			
		3,403,300	09/1968	Horowitz, et al.			
		3,515,949	06/1970	Michaels, et al.			
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		3,614,541	10/1971	Farrand			
		3,671,812	06/1972	Peluso, et al.			
		3,746,934	07/1973	Stein			
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		4,371,912	02/1983	Guzik			
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		4,398,235	08/1983	Lutz, et al.			
		4,571,663	02/1986	McPherson			
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		4,638,348	01/1987	Brown, et al.			
		4,638,406	01/1987	Samson			

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EXAMINER

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*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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	4,642,735	02/1987	Hodsdon, et al.			
	4,688,864	08/1987	Sorel			
	4,696,525	09/1987	Coller			
	4,698,663	10/1987	Sugimoto, et al.			
	4,706,166	11/1987	Go			
	4,761,681	08/1988	Reid			
	4,770,640	09/1988	Walter			
	4,821,007	04/1989	Fields, et al.			
	4,841,355	06/1989	Parks			
	4,868,712	09/1989	Woodman			
	4,884,237	11/1989	Mueller, et al.			
	4,924,352	05/1990	Septfons			
	4,953,005	08/1990	Carlson, et al.			
	4,956,694	09/1990	Eide			
	4,996,583	02/1991	Hatada			
	4,996,587	02/1991	Hinrichsmeyer, et al.			
	5,016,138	05/1991	Woodman			
	5,025,307	06/1991	Ueda, et al.			
	5,031,072	07/1991	Malhi, et al.			
	5,041,395	08/1991	Steffen			
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	5,058,265	10/1991	Goldfarb			
	5,086,018	02/1992	Conru, et al.			
	5,107,328	04/1992	Kinsman			
	5,128,831	07/1992	Fox, III, et al.			
	5,140,745	08/1992	McKenzie, Jr.,			
	5,155,068	10/1992	Tada			

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(USE SEVERAL SHEETS IF NECESSARY)

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Mark MoshayediFILING DATE
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2811**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		5,198,888	03/1993	Sugano, et al.			
		5,222,014	06/1993	Lin			
		5,231,304	07/1993	Solomon			
		5,239,447	08/1993	Cotues, et al.			
		5,241,454	08/1993	Ameen, et al.			
		5,281,852	01/1994	Normington			
		5,311,401	05/1994	Gates, Jr., et al.			
		5,313,096	05/1994	Eide			
		5,343,075	08/1994	Nishino			
		5,343,366	08/1994	Cipolla, et al.			
		5,369,058	11/1994	Burns, et al.			
		5,373,189	12/1994	Massit, et al.			
		5,384,689	01/1995	Shen			
		5,397,916	03/1995	Normington			
		5,420,751	05/1995	Burns			
		5,426,566	06/1995	Beilstein, Jr., et al.			
		5,446,313	08/1995	Masuda, et al.			
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		5,499,160	03/1996	Burns			
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		5,552,963	09/1996	Burns			
		5,561,591	10/1996	Burns			
		5,566,051	10/1996	Burns			
		5,586,009	12/1996	Burns			

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		5,605,592	02/1997	Burns			
		5,612,570	03/1997	Eide, et al.			
		5,615,475	04/1997	Burns			
		5,723,903	03/1998	Basuda, et al.			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		0 220 460 A2	09/1986	Europe				
		2 645 681	10/1990	France				
		30 984	03/1966	Germany			X	
		52-75981	12/1975	Japan				
		58-32440	02/1983	Japan				
		58-42247	03/1983	Japan				
		58-219757	12/1983	Japan				
		59-66154	04/1984	Japan				
		59-105345	06/1984	Japan				
		59-194460	11/1984	Japan				
		60-160641	08/1985	Japan				
		60-194548	10/1985	Japan				
		60-254762	12/1985	Japan				
		61-63048	04/1986	Japan				
		61-75558	04/1986	Japan				
		61-101067	05/1986	Japan				
		61-137335	06/1986	Japan				
		61-194753	08/1986	Japan				
		62-195138	08/1987	Japan				
		63-18654	01/1988	Japan				

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							YES	NO
		2-260448	10/1990	Japan				
		3-96266	04/1991	Japan				
		4-209562	07/1992	Japan				
		5-13666	01/1993	Japan				
		5-29540	05/1993	Japan			X	
		6-45501	02/1994	Japan				
		6-77644	03/1994	Japan			X	
		7-122842	05/1995	Japan				

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)	
	1	Patent Abstract of Japan, Publication No. 05029534, Published May 2, 1993, Inventor, Nakamura Shigemi, entitled "Memory Module", European Patent Office.
	2	"Alternative assembly for memory ICs," XP-002093051, Electronic Engineering, Jan. 1987, p. 22.
	3	International Electronic Device Meeting, IEDM Technical Digest, Washington, D.C., Dec. 6-9, 1987.
	4	3-D Integrated Packaging and Interconnect Technology, Wescon/90 Conference Record, held Nov. 13-15, 1990, Anaheim, CA.
	5	Tuckerman, D.B., et al., "Laminated Memory: A New 3-Dimensional Packaging Technology for MCMs" article, nCHIP, Inc., IEEE, 1994.
	6	1992 Proceedings, 42nd Electronic Components & Technology Conference, May 18-29, 1992.
	7	Dense-Pac Microsystems, 16-Megabit High Speed CMOS SRAM.
	8	Dense-Pac Microsystems, 128-Megabyte SDRAM Sodimm.
	9	Dense-Pac Microsystems, 256-Megabyte CMOS DRAM.
	10	Dense-Pac Microsystems, "While others are still defining it ... Our customers are cashing in!" flyer.
	11	IBM Technical Disclosure Bulletin, Vertical Chip Packaging, Vol. 20, No. 11A, Apr. 1978.
	12	IBM Technical Disclosure Bulletin, Edge-Mounted MLC Packaging Scheme, Vol. 23, No. 12, May 1981.
	13	IBM Technical Disclosure Bulletin, Process for Producing Lateral Chip Connectors, vol. 32, No. 3B, Aug. 1989.
	14	Research Disclosure, Organic Card Device Carrier, 31318, May 1990, No. 313.
	15	Dense-Pac Microsystems, "3-D Technology," 1993, 15 pages.
	16	Dense-Pac Microsystems, Inc., "Short Form Catalog," 1991, 20 pages.
	17	"New levels of hybrid IC density are provided by Three-Dimensional Packaging" article, 2 pages.

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18	Dense-Pac Microsystems, Inc., "Short Order Catalog," 1990, 12 pages.
19	Dense-Pac Microsystems, Inc., "Memory Products-Short Form-Q4," 1994, 5 pages.
20	"Electronic Packaging & Production" article, A Cahnners Publication, Jan. 1992, 2 pages.
21	"Introducing a Revolutionary 3 Dimensional Package Type-The SLCC," John Forthun, Advancement In Technology, Feb. 26, 1992, 12 pages.
22	Dense-Pac Microsystems, Inc., 256KX1BASED CMOS SRAM Family - Preliminary, 1988/89.
23	Dense-Pac Microsystems, Inc., DPS256X16A3 Ceramic 256K x 16 CMOS RAM Module, 1991.
24	Dense-Pac Microsystems, Inc., DPS128X24AV3, High Speed 128K x 24 CMOS SRAM Versa-stack, 1991.
25	Dense-Pac Microsystems, Inc., 8 Magabit CMOS SRAM, DPS256S32W, 1994.
26	Dense-Pac Microsystems, Inc., 128 Megabit CMOS DRAM, DPD16MX8PH4, 1994.

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